HW-SW ICD

OTS

Rev 1.0

|  |  |  |  |
| --- | --- | --- | --- |
| R E V I S I O N S | | | |
| **REV.** | **DESCRIPTION** | **RELEASE DATE** | **CHANGES DESCRIPTION** |
| 1 |  | 22/12/2019 | First Release |
|  |  |  |  |
|  |  |  |  |

The following document describes the connections and functionality of peripheral devices, connected to the MCU

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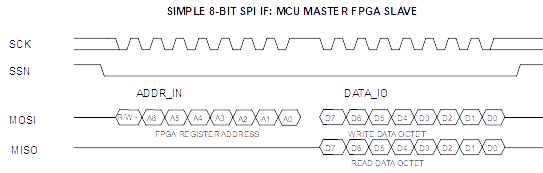
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# FPGA

SPI is 8bit rising edge normally 1



|  | | | |
| --- | --- | --- | --- |
| Register Address Offset (Hex) | Description |  |  |
| 0x00 | Hardware Revision Register |  |  |
| 0x04 | Test register |  |  |
| 0x10 | B\_in Discrete register |  |  |
| 0x14 | C\_in Discrete register |  |  |
| 0x18 | C\_out Discrete register |  |  |
| 0x1C | Spare discrete register |  |  |
| 0x20 | Discrete Control register |  |  |
| 0x24 | Discrete Test register1 |  |  |
| 0x28 | Discrete Test register2 |  |  |
| 0x2C | Board Voltage Measure1 |  |  |
| 0x30 | Board Voltage Measure2 |  |  |
| 0x34 | Board Voltage Measure3 |  |  |
| 0x38 |  |  |  |
| 0x3C |  |  |  |
| 0x40 |  |  |  |
| 0x44 | OPT\_ADC\_TEMP |  |  |
| 0x48 | OPT\_ADC\_DIODE\_PWR |  |  |
| 0x4C | OPT\_ADC\_OUT\_PWR |  |  |
| 0x50 | OPT\_DAC\_LASER\_OFF |  |  |
| 0x54 | OPT\_DAC\_MOD\_BIAS |  |  |
| 0x58 | RF\_ADC\_DETECT1 |  |  |
| 0x5C | RF\_ADC\_DETECT2 |  |  |
| 0x60 | RF\_DAC\_VGS2 |  |  |
|  |  |  |  |

## Test\_Register

Address 0, Read & Write

Value previously written into this register can be written.

## Hardware Revision Register

Address 1, Read Only

Read current hardware revision.

## Discretes Out Bit Register

Address 2, Read Only

Read back output discretes values for BIT.

D7-D5 Constant "000"

D4 LBJP\_TI\_LB\_BIT discrete test value read

D3 LBJP\_TI\_MB\_BIT discrete test value read

D2 LBJP\_RI\_LB\_BIT discrete test value read

D1 LBJP\_RI\_MB\_BIT discrete test value read

D0 CDFRALBJP\_BIT discrete test value read

## Discretes In Read Register

Address 3, Read Only

Read current hardware revision.

D7-D4 Constant "0000"

D3 LBJP\_TR\_LB discrete value read

D2 LBJP\_RW\_LB discrete value read

D1 LBJP\_TR\_MB discrete value read

D0 LBJP\_RW\_MB discrete value read

## Serdes\_SFP\_Status Register

Address 4, Read Only

Read current hardware revision.

` D7-D2 Constant "000000"

D1 SER1\_TXFLT ‘1’ means the SERDES SFP failed to transmit to optical link due to error.

D0 SER1\_LOS ‘1’ means the SERDES SFP doesn’t see optical energy

## Leds Register

Address 16, Write Only

Write to LEDs On Board

D4 Write to LED4, ‘0’ is “ON”

D3 Write to LED3, ‘0’ is “ON”

D2 Write to LED2, ‘0’ is “ON”

D1 Write to LED1, ‘0’ is “ON”

D0 Write to LED0, ‘0’ is “ON”

## SERDES Control Register

Address 17, Write Only

Control signals to discretes SERDES chip – see TLK2501 Data Sheet.

D5 SER1\_PRBSEN ‘1’ Send PRBS instead data

D4 SER1\_LOCREFN ‘1’ Lock On RX Channel

D3 SER1\_ENABLE ‘1’ Serializer Enable

D2 SER1\_TX\_ER ‘1’ Insert Error To TX Transmission

D1 SER1\_LOOPEN ‘1’ Make Internal Loopback TX to RX

D0 SER1\_TXDIS ‘1’ Transmit Disable.

# Non FPGA

## Debug UART

LVCMOS 3.3V UART

DBG\_UART\_TX MCU PA9

DBG\_UART\_RX MCU PA10

## External UART

LVCMOS 3.3V UART

UART\_TX MCU PD5

UART\_RX MCU PD6

## Ethernet P0 SFP Control

P0\_S\_TXDIS MCU PE3 Write – Transmit Disable

P0\_S\_TXFLT MCU PE4 Read – TX Faulte detected

P0\_S\_LOS MCU PE5 Read – RX LOS was detected

## Serial FLASH

See M24512-DRDW3TP data sheet

EE\_SCL MCU PB8

EE\_SDA MCU PB9

## Onboard LEDs

“0” is ON

LED1 MCU PI0

LED2 MCU PI2

LED3 MCU PI9

LED4 MCU PI11